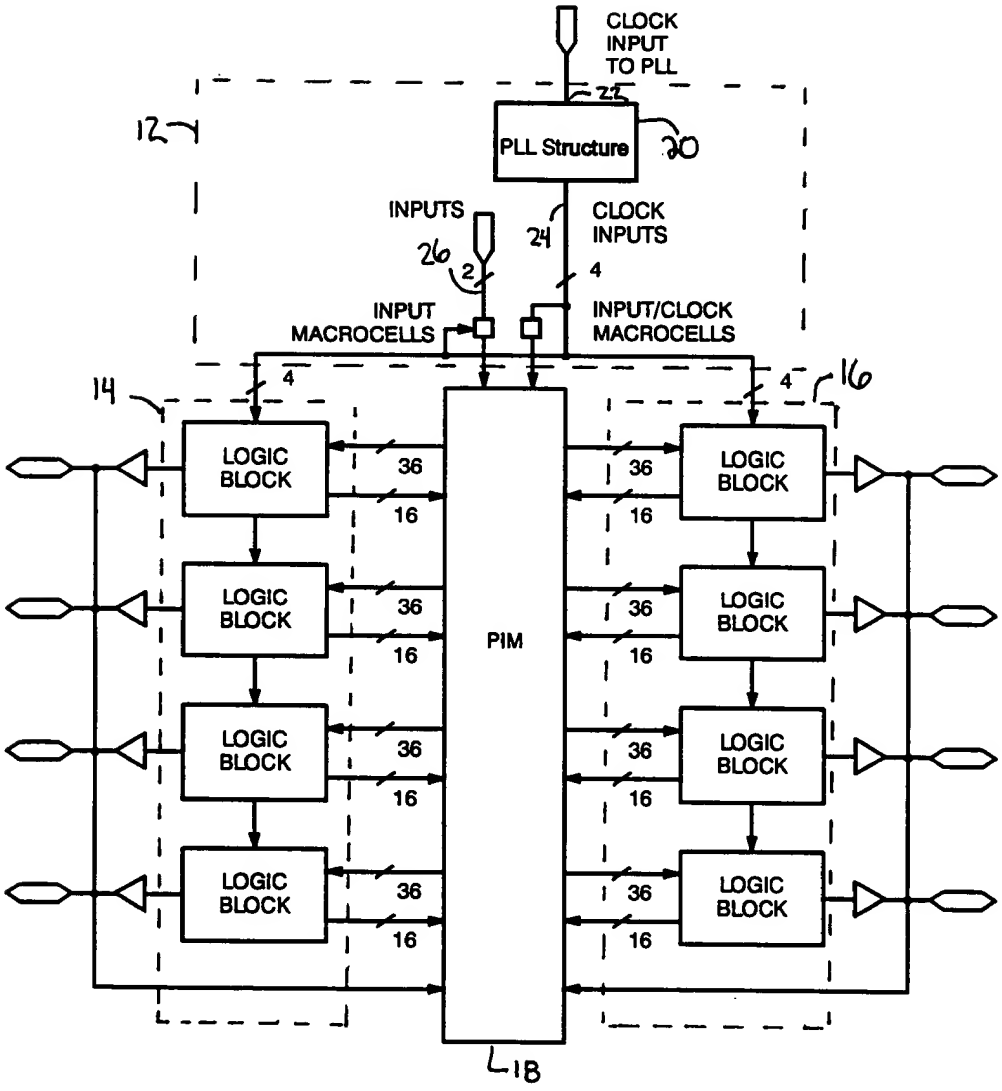
CLOCK
INPUT
TO PLL
22
12
PLL Structure
20
INPUTS
26
2
24
CLOCK
INPUTS
4
INPUT
MACROCELLS
INPUT/CLOCK
MACROCELLS
14
4
4
16
LOGIC
BLOCK
36
16
PIM
18

FIG. 1

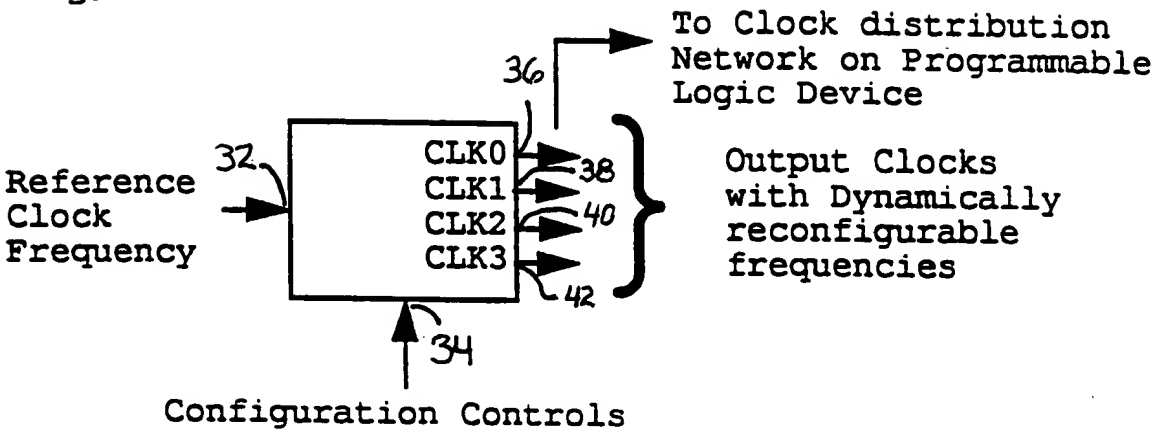

FIG. 2

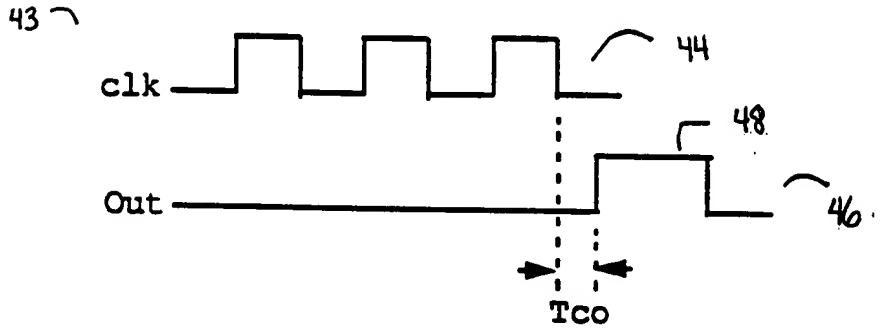

FIG. 3

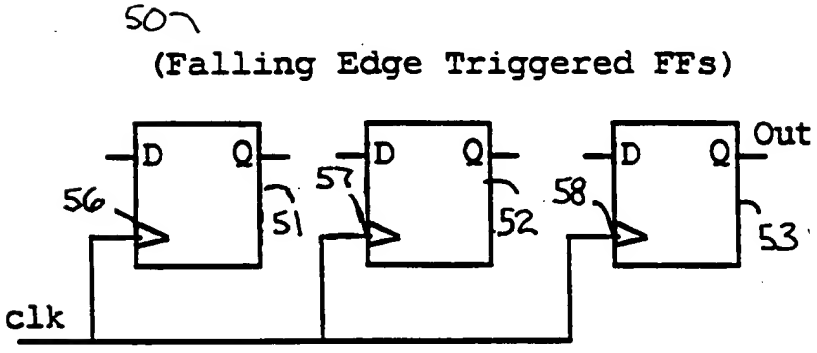

FIG. 4

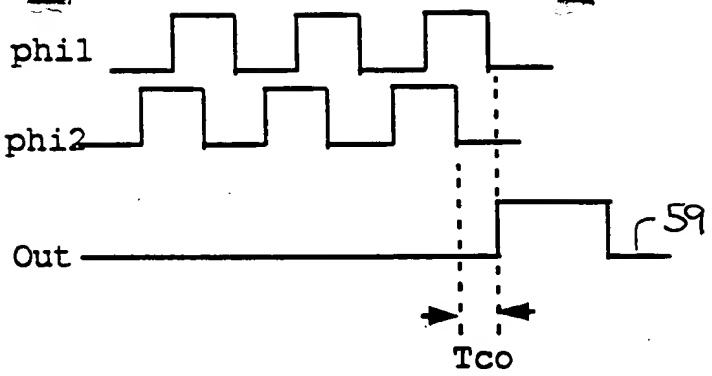

FIG. 5

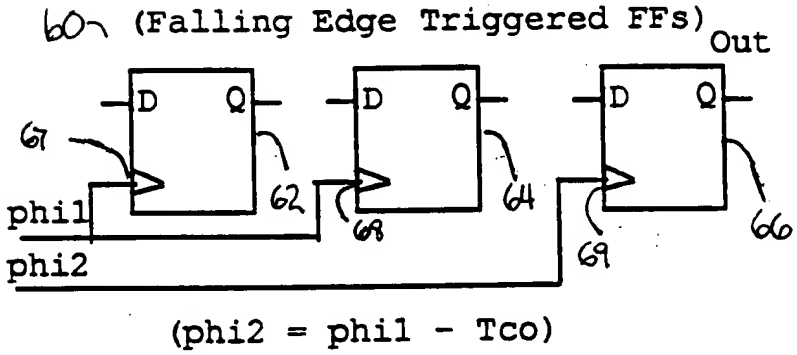

FIG. 6

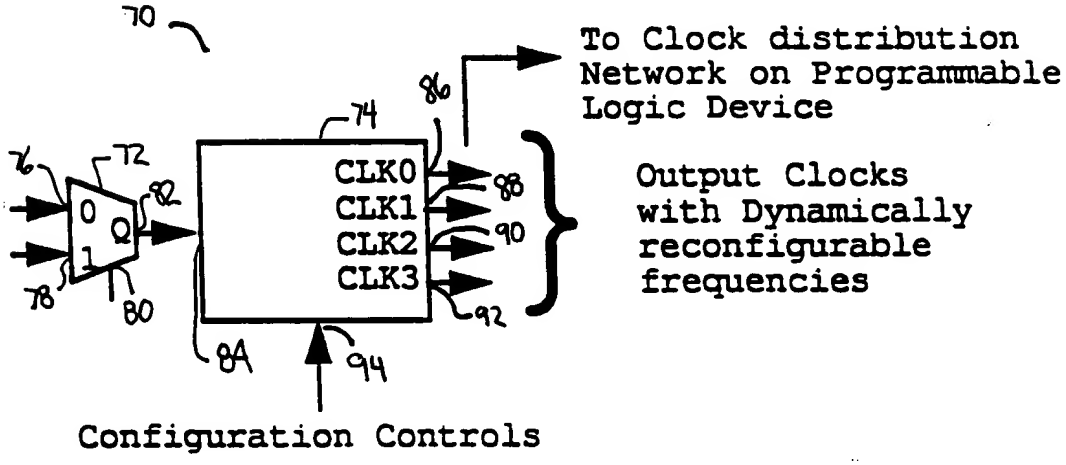

FIG. 7